

signalling between different chips and modules, the prior art requires the use of connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling non-conductively, for example, either capacitively or magnetically. Preferably, pairs of half-capacitor plates, one half located on each chip, module or substrate are used to capacitively couple signals from one chip, module or substrate to another. The use of plates relaxes the need for high precision alignment as well as reduces the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

In response to the office action, applicants have amended independent claim 28 and added claims 206-209 dependent on claim 28 to overcome the § 112 rejection and to more particularly point out and distinctly claim the subject matter that applicants regard as their invention. Applicants appreciate the indication of allowable subject matter in claim 144 but believe that independent claim 102 patentably distinguishes applicants' invention over the prior art.

Further, claims 3-12 were incorrectly withdrawn from consideration by the Examiner. Claims 3-12 are among the claims applicants elected in response to the restriction requirement of 10/17/95. Accordingly, applicants request that claims 3-12 be addressed on the merits in the next action.

Also, claims 29, 80-101, and 201-202 were canceled in response to the restriction requirement dated May 15, 1995 but were indicated by the Examiner in the most recent action as being only withdrawn from consideration. Applicants request that these claims be canceled as indicated in our previous response.

Applicants continue to traverse the way the Examiner has specified the species in paragraph 1 of the restriction requirement as follows:

c) The embodiment of subparagraph (c) (figure 3) is not distinct from that of subparagraph (a). Page 26, line 20 of the specification indicates that die 11 of figure 1 includes

conductive contacts 16 for powering device 12. At lines 26-28 and with reference to figure 1, the specification indicates that power could be provided "by means of a metallic fuzz button." Figure 3 shows a modular electronic system including metallic fuzz buttons 41, 42, 43 that contact conductive contact pads 45, 46, 47. The discussion of figure 3 also indicates at page 33, lines 30-34 several alternatives for these conductive means.

e) The embodiment of subparagraph(e) is clearly not a waveform. As indicated in the specification at page 36, line 21, it is a MCM similar to that of figure 4.

f) The diagrams of figure 6 are not an embodiment at all but waveforms illustrative of signals coupled between dies 11 and 85 of figure 5 as stated at page 41, line 32.

g and h) The embodiments of subparagraphs g and h(figures 8,9, and 10) are not distinct from those of subparagraph (a). The embodiments of figures 8,9, and 10 are simply more complicated structures extending the same principles set forth in the embodiment of figure 1. See, for example, the discussion of figure 1 at page 26, lines 4-9 and page 32, lines 15-25.

i) Figures 11a,11b,12a, and 12b explain the advantage of the present invention(its ability to compensate for misalignment) and are not the description of a separate embodiment.

j) Figure 13 is not described in the specification as illustrating a superconductor structure. Rather, it is a multi-level structure to which the comments on subparagraphs g and h are applicable. Figure 14 does illustrate a superconducting device. However, figure 14 is not distinct from the embodiment of subparagraph (a) which contemplates at page 27, line 11, the use of a superconducting substrate.

l) The method claims in the present application have been canceled.

n) The embodiments of subparagraph (n)(Figures 20a-b) are not distinct from those of subparagraph (a). The embodiments of subparagraph (n) are application specific modules. Module 277a of figure 15 which is part of the

species of subparagraph (a) is identified at page 54, line 31 as being a custom ASIC(application specific integrated circuit) die.

r and s) The method claims have been canceled from the present invention.

Applicants are unable to reconcile apparent inconsistencies in the Examiner's determination of species. For example, claim 9 is associated with both the species of subparagraph (a) and that of subparagraph (c). Claims 10, 11, and 12, which are dependent on claim 9 are associated with the species of subparagraph (a) but not that of subparagraph (c). Dependent claim 4 which is drawn to an ASIC is associated with the species of subparagraph (a) but not that of subparagraph (n) which is also an ASIC. Further, it is not understood why some of the claims(e.g., claims 5,6, and 7) are deemed to be readable on the species of subparagraph (a) while numerous others are not.

Applicants also traverse the Examiner's statement in paragraph 2 that there are no generic claims in the application. For example, claim 1 reads on not only the embodiments of figures 1,7, and 15 but also those of at least figures 3,4,5,14,20b, and 22. Claims 28 and 102 read on all embodiments in which capacitive coupling is employed.

In response to the requirement to list all claims readable on the elected species(subparagraph (a))(figures 1,7, and 15), applicants continue to submit that at least the following claims are readable thereon in view of the broad teaching in the specification of the interchangeability of various features of the invention among the various embodiments disclosed and the lack of distinction among certain alleged species as described above: Claims 1-13,15-25,28,36-68,70-79,102-111,113-129,136-158,161-196, and 199-200.

Applicants respectfully submit that the Examiner misapprehends what is meant by "capacitively signalling" between different chips and substrates. A capacitor consists of two metal plates separated by an insulator and its so-called characteristic property - capacitance - is the ratio of

the charge on the plates to the potential difference between the plates. In the prior art, capacitors are used within a single chip or circuit to couple a signal from one node to another, such as for filtering, tuning, DC blocking, or energy storage. As indicated by Howard, capacitors are also used extensively to reduce voltage fluctuations on power and ground planes. Applicants do not claim that this is their invention. Rather, applicants have discovered that capacitively coupling a signal between different chips, modules, or substrates that are distinct and separate from one another obviates the need for physical connectors.

In contrast to applicants' invention, Howard's invention is directed towards resolving the prior art's shortcomings in compensating for voltage fluctuations arising between power and ground planes (See column 1, lines 27-61). Howard et al. disclose a capacitor laminate 26 formed from a power plane 28 and a ground plane 30 and separated by a dielectric sheet 32. The chips 14 receive power from the capacitor laminate 26 via power leads 34 and 36. In sum, Howard's invention merely discloses a method of sharing capacitive power and ground planes among a plurality of chips 14 and in no way anticipates or renders obvious applicants' invention of capacitively signalling between different chips and substrates.

With respect to claim 1, Howard does not show "means for capacitively signalling between said chip 14 and said substrate 10." That is, the capacitive laminates 26, 26', 40, 42 disclosed by Howard are formed by the ground and power planes (See column 11, lines 58-60 and column 12, lines 35-50 and lines 62-68) and thus do not and can not perform a "signalling" function as the planes merely provide a constant voltage shared among a plurality of chips 14.

Examiner contends that the Abstract teaches "means for capacitively signalling between the chip 14 and the substrate 10." However, the Abstract merely indicates that the capacitive laminates 26 are shared by a large number of devices on the PCB. As indicated above, the specification clearly indicates that these shared capacitive laminates 26 are implemented exclusively as power and ground planes.

Indeed, the shared capacitive elements 26 could not be used as signal paths as the chips 14 connected to them operate randomly (see col 9, lines 6-8). Clearly, sharing signal paths in an asynchronous environment would inevitably result in signal interference.

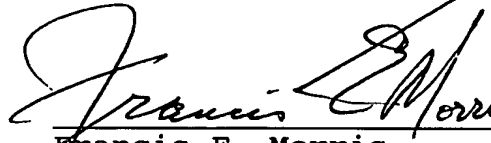
Claim 28 as amended recites "a chip; a substrate; a plurality of electronic devices implemented on said chip, at least one of said plurality of electronic devices coupled to a first half-capacitor attached to said chip; and, a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor." Such language patentably distinguishes the claimed invention from the prior art. Namely, Howard does not disclose a second half-capacitor "capacitively coupling a signal to said first half-capacitor" as is presently claimed.

With respect to independent claim 102, applicants respectfully disagree with the Examiner's characterization of the substrate 10 shown in Howard's figure 5. As best applicants can tell, the Examiner's position is that everything in substrate 10' above plane 28' of laminate 40 is in a first module A and everything in substrate 10' below plane 30' of laminate 40 is in a second module B. Applicants fail to understand how Howard's substrate 10 can reasonably be construed to have first and second "modules" because element 40 is described as a laminate of power and ground planes 28' and 30' and dielectric sheet 32' which suggests that it is an essentially integral structure. In any event, figure 5 does not show first and second half-capacitors that "provide a capacitive signal path between the first and second modules" as is claimed. As discussed above, Howard's capacitive laminates are formed by ground and power planes and these cannot be construed as providing signal paths.

For these reasons, applicants believe that the grounds of rejection are overcome and respectfully request the Examiner to pass the subject application to issue.

Respectfully submitted,

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Enclosure